INTEGRATION OF HIGH K GATE DIELECTRIC

Abstract of the Disclosure

Methods are provided herein for forming electrode layers over high dielectric constant ("high k") materials. In the illustrated embodiments, a high k gate dielectric, such as zirconium oxide, is protected from reduction during a subsequent deposition of silicon-containing gate electrode. In particular, a seed deposition phase includes conditions designed for minimizing hydrogen reduction of the gate dielectric, including low hydrogen content, low temperatures and/or low partial pressures of the silicon source gas. Conditions are preferably changed for higher deposition rates and deposition continues in a bulk phase. Desirably, though, hydrogen diffusion is still minimized by controlling the above-noted parameters. In one embodiment, high k dielectric reduction is minimized through omission of a hydrogen carrier gas. In another embodiment, a higher order silanes, such as disilane and trisilane, aid in reducing hydrogen content for a given deposition rate.